To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35054-XXXFP/M35055-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35054-XXXFP and M35055-XXXFP are TV screen display control IC which can be used to display information such as number of channels, the date and messages and program schedules on the TV screen.

In particular, owing to the built-in SYNC-SEP (synchronous separation) circuit, the synchronous correction circuit, external circuits can be decrease and character turbulence that occurs when superimposing can be reduced. The processor is suitable for AV systems such as VTRs, LDs, and so on.

It is a silicon gate CMOS process and M35054-XXXFP and M35055-XXXFP are housed in a 20-pin shrink SOP package.

For M35054-001FP/M35055-001FP that are a standard ROM versions of M35054-XXXFP/M35055-XXXFP respectively, the character pattern is also mentioned.

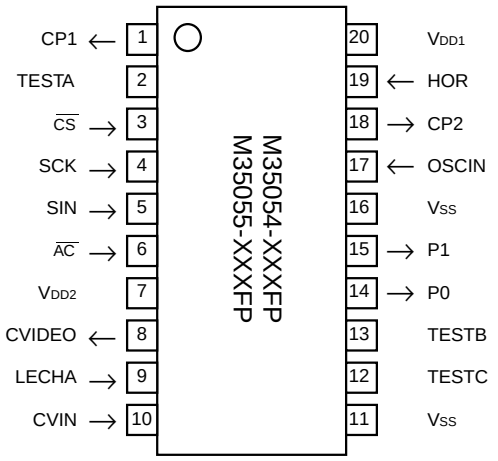
FEATURES

- Screen composition ..... 24 characters × 10 lines, 32 characters × 7 lines
- Number of characters displayed ..... 240 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 128 characters (M35054)
  ..... 256 characters (M35055)
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  Horizontal direction ..... 240 locations
  Vertical direction ..... 256 locations
- Blinking ..... Character units
  Cycle : approximately 1 second, or approximately 0.5 seconds
  Duty : 25%, 50%, or 75%
- Data input ..... By the serial input function (16 bits)
- Coloring
  Background coloring (composite video signal)
- Blanking
  Total blanking (14 × 18 dots)
  Border size blanking
  Character size blanking
- Synchronizing signal
  Composite synchronizing signal generation
  (PAL, NTSC, M-PAL)
- 2 output ports (1 digital line)
- Oscillation stop function
  It is possible to stop the oscillation for synchronizing signal generation
- Built-in half-tone display function
- Built-in reversed character display function
- Built-in synchronous correction circuit
- Built-in synchronous separation circuit

APPLICATION

TV, VCR, Movie

PIN CONFIGURATION (TOP VIEW)



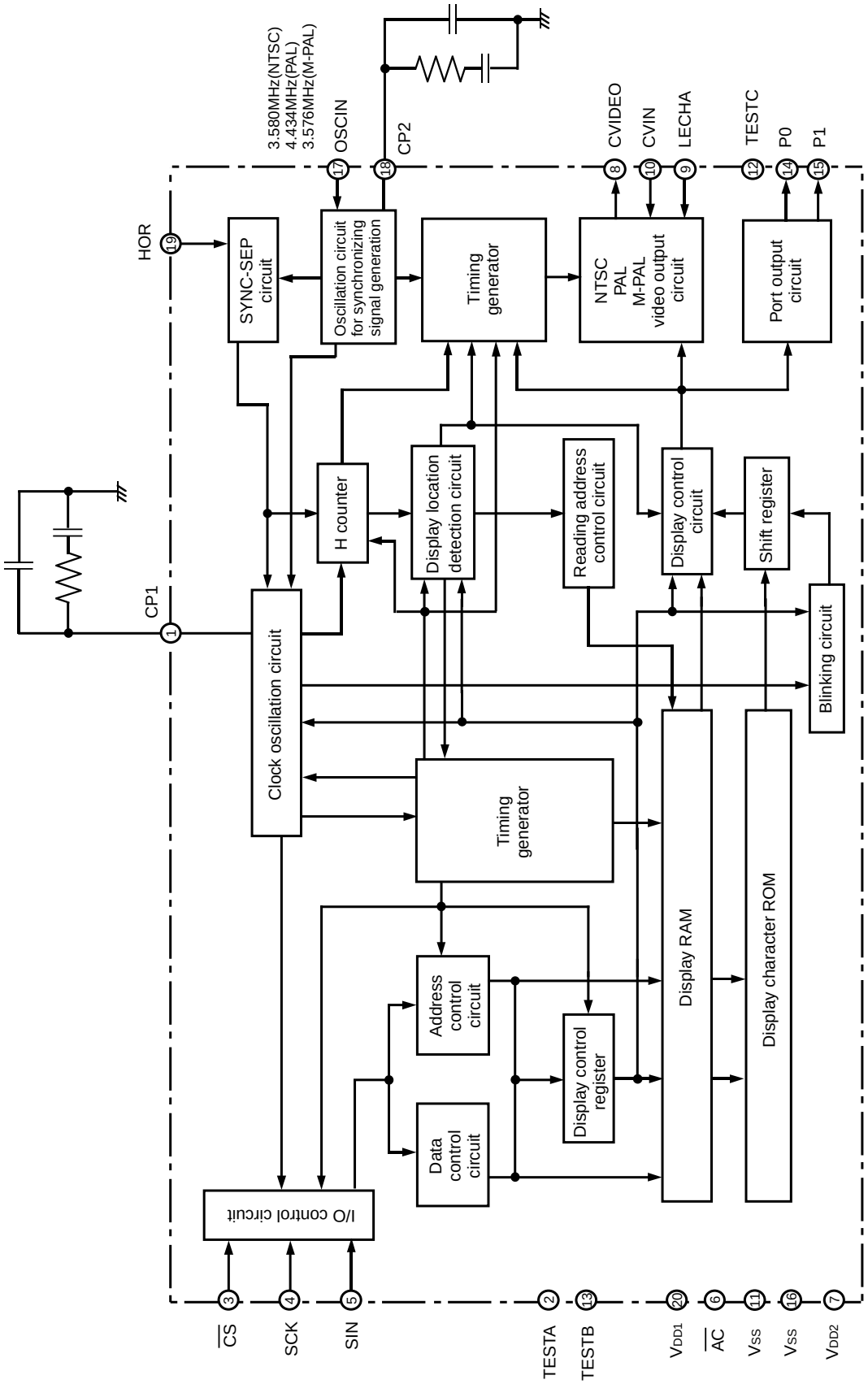
Outline 20P2Q-A

RENESAS
Renesas Technology Corp.

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
OSC1	Clock input	Input	This is the filter output pin 1.
TESTA	Test pin input	—	This is the pin for test. Connect this pin to GND during normal operation.
$\overline{CS}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to “L”. Hysteresis input. Built-in pull-up resistor.
SCK	Serial clock input	Input	When $\overline{CS}$ pin is “L”, SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor.
SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Built-in pull-up resistor.
$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
V_{DD2}	Power pin	—	Please connect to +5V with the analog circuit power pin.
CVIDEO	Composite video signal output	Output	This is the output pin for composite video signals. It outputs $2V_{P-P}$ composite video signals. In superimpose mode, character output etc. is superimposed on the external composite video signals from CVIN.
LECHA	Character level input	Input	This is the input pin which determines the “white” character color level in the composite video signal.
CVIN	Composite video signal input	Input	This is the input pin for external composite video signals. In superimpose mode, character output etc. is superimposed on these external composite video signals.
V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin.
TESTC	Test pin output	—	This is the pin for test. Open this pin during normal operation.
TESTB	Test pin input	—	This is the pin for test. Connect this pin to GND during normal operation.
P0	Port P0 output	Output	This pin outputs the port output or BLNK1 (character background) signal.
P1	Port P1 output	Output	This pin outputs the port output or CO1(character) signal.
V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin (Analog side).
OSCIN	f_{SC} input pin for synchronous signal generation	Input	This is the input pin for the sub-carrier frequency (f_{SC}) for generating a synchronous signal. A frequency of 3.580MHz is needed for NTSC, and a frequency of 4.434MHz in needed for PAL and 3.576MHz is needed for M-PAL.
CP2	Filter output	Output	Filter output pin 2.
HOR	Horizontal synchro-nizing signal input	Input	This is the input pin for external composite video signals. This pin inputs the external video signal clamped sync-chip to 1.5V, and internally carries out synchronous separa-tion.
V_{DD1}	Power pin	—	Please connect to +5V with the digital circuit power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 00_{16} to EF_{16} are assigned to the display RAM, address $F0_{16}$ to $F8_{16}$ are assigned to the display control registers.

The internal circuit is reset and all display control registers (address $F0_{16}$ to $F8_{16}$) are set to “0” and display RAM (address 00_{16} to EF_{16}) are RAM erased when the $\overline{AC}$ pin level is “L”.

When using M35054-XXXFP, set “0” in any of DA7, DAD through DAF of addresses 00_{16} through EF_{16}, and of DAE and DAF of addresses $F0_{16}$ through $F8_{16}$.

Setting the blank code “FF_{16}” as a character code is an exception.

When using M35055-XXXFP, set “0” in any of DAD through DAF of addresses 00_{16} through EF_{16}, and of DAE and DAF of addresses $F0_{16}$ through $F8_{16}$.

TESTn (n : a number) is MITSUBISHI test memory, so be sure to observe the setting conditions.

Address		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00_{16}	Display RAM	0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
⋮		⋮	⋮	⋮	Reverse	Blinking	Character color			⋮	Character code						
EF_{16}		0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
$F0_{16}$	Display control register	0	0	TEST15	TEST14	TEST13	TEST12	TEST11	TEST10	SYSEP1	SYSEP0	SEPV1	SEPV0	PTD1	PTD0	PTC1	PTC0
$F1_{16}$		0	0	TEST21	TEST20	TEST19	TEST18	TEST17	TEST16	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
$F2_{16}$		0	0	TEST27	TEST26	TEST25	TEST24	TEST23	TEST22	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
$F3_{16}$		0	0	TEST33	TEST32	TEST31	TEST30	TEST29	TEST28	VSZ21	VSZ20	VSZ11	VSZ10	HSZ21	HSZ20	HSZ11	HSZ10
$F4_{16}$		0	0	TEST36	TEST35	TEST34	SPACE	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
$F5_{16}$		0	0	TEST42	TEST41	TEST40	TEST39	TEST38	TEST37	EQP	PALH	MPAL	$\overline{INT}$/NON	$\overline{N}$/P	BLINK2	BLINK1	BLINK0
$F6_{16}$		0	0	TEST43	TEST2	TEST1	TEST0	LBLACK	LIN$\overline{24}$/32	BLKHF	BB	BG	BR	LEVEL0	PHASE2	PHASE1	PHASE0
$F7_{16}$		0	0	TEST46	TEST45	RGBON	TEST44	CL$\overline{17}$/18	CBLINK	CURS7	CURS6	CURS5	CURS4	CURS3	CURS2	CURS1	CURS0
$F8_{16}$		0	0	LEVEL1	TEST51	TEST50	TEST49	TEST48	TEST47	RAMERS	DSPON	STOP1	STOPIN	SCOR	EX	BLK1	BLK0

Fig. 1 Memory constitution (M35054-XXXFP)

Address		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00_{16}	Display RAM	0	0	0	REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮		⋮	⋮	⋮	Reverse	Blinking	Character color			Character code							
EF_{16}		0	0	0	REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
$F0_{16}$	Display control register	0	0	TEST15	TEST14	TEST13	TEST12	TEST11	TEST10	SYSEP1	SYSEP0	SEPV1	SEPV0	PTD1	PTD0	PTC1	PTC0
$F1_{16}$		0	0	TEST21	TEST20	TEST19	TEST18	TEST17	TEST16	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
$F2_{16}$		0	0	TEST27	TEST26	TEST25	TEST24	TEST23	TEST22	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
$F3_{16}$		0	0	TEST33	TEST32	TEST31	TEST30	TEST29	TEST28	VSZ21	VSZ20	VSZ11	VSZ10	HSZ21	HSZ20	HSZ11	HSZ10
$F4_{16}$		0	0	TEST36	TEST35	TEST34	SPACE	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
$F5_{16}$		0	0	TEST42	TEST41	TEST40	TEST39	TEST38	TEST37	EQP	PALH	MPAL	$\overline{INT}$/NON	$\overline{N}$/P	BLINK2	BLINK1	BLINK0
$F6_{16}$		0	0	TEST43	TEST2	TEST1	TEST0	LBLACK	LIN$\overline{24}$/32	BLKHF	BB	BG	BR	LEVEL0	PHASE2	PHASE1	PHASE0
$F7_{16}$		0	0	TEST46	TEST45	RGBON	TEST44	CL$\overline{17}$/18	CBLINK	CURS7	CURS6	CURS5	CURS4	CURS3	CURS2	CURS1	CURS0
$F8_{16}$		0	0	LEVEL1	TEST51	TEST50	TEST49	TEST48	TEST47	RAMERS	DSPON	STOP1	STOPIN	SCOR	EX	BLK1	BLK0

Fig. 2 Memory constitution (M35055-XXXFP)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen consitution (24 characters × 10 lines) is shown in Figure 3 the screen constitution (32 characters × 7 lines) is shown in 4.

Lines \ Rows	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00_{16}	01_{16}	02_{16}	03_{16}	04_{16}	05_{16}	06_{16}	07_{16}	08_{16}	09_{16}	$0A_{16}$	$0B_{16}$	$0C_{16}$	$0D_{16}$	$0E_{16}$	$0F_{16}$	10_{16}	11_{16}	12_{16}	13_{16}	14_{16}	15_{16}	16_{16}	17_{16}
2	18_{16}	19_{16}	$1A_{16}$	$1B_{16}$	$1C_{16}$	$1D_{16}$	$1E_{16}$	$1F_{16}$	20_{16}	21_{16}	22_{16}	23_{16}	24_{16}	25_{16}	26_{16}	27_{16}	28_{16}	29_{16}	$2A_{16}$	$2B_{16}$	$2C_{16}$	$2D_{16}$	$2E_{16}$	$2F_{16}$
3	30_{16}	31_{16}	32_{16}	33_{16}	34_{16}	35_{16}	36_{16}	37_{16}	38_{16}	39_{16}	$3A_{16}$	$3B_{16}$	$3C_{16}$	$3D_{16}$	$3E_{16}$	$3F_{16}$	40_{16}	41_{16}	42_{16}	43_{16}	44_{16}	45_{16}	46_{16}	47_{16}
4	48_{16}	49_{16}	$4A_{16}$	$4B_{16}$	$4C_{16}$	$4D_{16}$	$4E_{16}$	$4F_{16}$	50_{16}	51_{16}	52_{16}	53_{16}	54_{16}	55_{16}	56_{16}	57_{16}	58_{16}	59_{16}	$5A_{16}$	$5B_{16}$	$5C_{16}$	$5D_{16}$	$5E_{16}$	$5F_{16}$
5	60_{16}	61_{16}	62_{16}	63_{16}	64_{16}	65_{16}	66_{16}	67_{16}	68_{16}	69_{16}	$6A_{16}$	$6B_{16}$	$6C_{16}$	$6D_{16}$	$6E_{16}$	$6F_{16}$	70_{16}	71_{16}	72_{16}	73_{16}	74_{16}	75_{16}	76_{16}	77_{16}
6	78_{16}	79_{16}	$7A_{16}$	$7B_{16}$	$7C_{16}$	$7D_{16}$	$7E_{16}$	$7F_{16}$	80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}	88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$
7	90_{16}	91_{16}	92_{16}	93_{16}	94_{16}	95_{16}	96_{16}	97_{16}	98_{16}	99_{16}	$9A_{16}$	$9B_{16}$	$9C_{16}$	$9D_{16}$	$9E_{16}$	$9F_{16}$	$A0_{16}$	$A1_{16}$	$A2_{16}$	$A3_{16}$	$A4_{16}$	$A5_{16}$	$A6_{16}$	$A7_{16}$
8	$A8_{16}$	$A9_{16}$	AA_{16}	AB_{16}	AC_{16}	AD_{16}	AE_{16}	AF_{16}	$B0_{16}$	$B1_{16}$	$B2_{16}$	$B3_{16}$	$B4_{16}$	$B5_{16}$	$B6_{16}$	$B7_{16}$	$B8_{16}$	$B9_{16}$	BA_{16}	BB_{16}	BC_{16}	BD_{16}	BE_{16}	BF_{16}
9	$C0_{16}$	$C1_{16}$	$C2_{16}$	$C3_{16}$	$C4_{16}$	$C5_{16}$	$C6_{16}$	$C7_{16}$	$C8_{16}$	$C9_{16}$	CA_{16}	CB_{16}	CC_{16}	CD_{16}	CE_{16}	CF_{16}	$D0_{16}$	$D1_{16}$	$D2_{16}$	$D3_{16}$	$D4_{16}$	$D5_{16}$	$D6_{16}$	$D7_{16}$
10	$D8_{16}$	$D9_{16}$	DA_{16}	DB_{16}	DC_{16}	DD_{16}	DE_{16}	DF_{16}	$E0_{16}$	$E1_{16}$	$E2_{16}$	$E3_{16}$	$E4_{16}$	$E5_{16}$	$E6_{16}$	$E7_{16}$	$E8_{16}$	$E9_{16}$	EA_{16}	EB_{16}	EC_{16}	ED_{16}	EE_{16}	EF_{16}

Note : The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution (24 characters × 10 lines)

Lines \ Rows	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	00_{16}	01_{16}	02_{16}	03_{16}	04_{16}	05_{16}	06_{16}	07_{16}	08_{16}	09_{16}	$0A_{16}$	$0B_{16}$	$0C_{16}$	$0D_{16}$	$0E_{16}$	$0F_{16}$	10_{16}	11_{16}	12_{16}	13_{16}	14_{16}	15_{16}	16_{16}	17_{16}	18_{16}	19_{16}	$1A_{16}$	$1B_{16}$	$1C_{16}$	$1D_{16}$	$1E_{16}$	$1F_{16}$
2	20_{16}	21_{16}	22_{16}	23_{16}	24_{16}	25_{16}	26_{16}	27_{16}	28_{16}	29_{16}	$2A_{16}$	$2B_{16}$	$2C_{16}$	$2D_{16}$	$2E_{16}$	$2F_{16}$	30_{16}	31_{16}	32_{16}	33_{16}	34_{16}	35_{16}	36_{16}	37_{16}	38_{16}	39_{16}	$3A_{16}$	$3B_{16}$	$3C_{16}$	$3D_{16}$	$3E_{16}$	$3F_{16}$
3	40_{16}	41_{16}	42_{16}	43_{16}	44_{16}	45_{16}	46_{16}	47_{16}	48_{16}	49_{16}	$4A_{16}$	$4B_{16}$	$4C_{16}$	$4D_{16}$	$4E_{16}$	$4F_{16}$	50_{16}	51_{16}	52_{16}	53_{16}	54_{16}	55_{16}	56_{16}	57_{16}	58_{16}	59_{16}	$5A_{16}$	$5B_{16}$	$5C_{16}$	$5D_{16}$	$5E_{16}$	$5F_{16}$
4	60_{16}	61_{16}	62_{16}	63_{16}	64_{16}	65_{16}	66_{16}	67_{16}	68_{16}	69_{16}	$6A_{16}$	$6B_{16}$	$6C_{16}$	$6D_{16}$	$6E_{16}$	$6F_{16}$	70_{16}	71_{16}	72_{16}	73_{16}	74_{16}	75_{16}	76_{16}	77_{16}	78_{16}	79_{16}	$7A_{16}$	$7B_{16}$	$7C_{16}$	$7D_{16}$	$7E_{16}$	$7F_{16}$
5	80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}	88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$	90_{16}	91_{16}	92_{16}	93_{16}	94_{16}	95_{16}	96_{16}	97_{16}	98_{16}	99_{16}	$9A_{16}$	$9B_{16}$	$9C_{16}$	$9D_{16}$	$9E_{16}$	$9F_{16}$
6	$A0_{16}$	$A1_{16}$	$A2_{16}$	$A3_{16}$	$A4_{16}$	$A5_{16}$	$A6_{16}$	$A7_{16}$	$A8_{16}$	$A9_{16}$	AA_{16}	AB_{16}	AC_{16}	AD_{16}	AE_{16}	AF_{16}	$B0_{16}$	$B1_{16}$	$B2_{16}$	$B3_{16}$	$B4_{16}$	$B5_{16}$	$B6_{16}$	$B7_{16}$	$B8_{16}$	$B9_{16}$	BA_{16}	BB_{16}	BC_{16}	BD_{16}	BE_{16}	BF_{16}
7	$C0_{16}$	$C1_{16}$	$C2_{16}$	$C3_{16}$	$C4_{16}$	$C5_{16}$	$C6_{16}$	$C7_{16}$	$C8_{16}$	$C9_{16}$	CA_{16}	CB_{16}	CC_{16}	CD_{16}	CE_{16}	CF_{16}	$D0_{16}$	$D1_{16}$	$D2_{16}$	$D3_{16}$	$D4_{16}$	$D5_{16}$	$D6_{16}$	$D7_{16}$	$D8_{16}$	$D9_{16}$	DA_{16}	DB_{16}	DC_{16}	DD_{16}	DE_{16}	DF_{16}

Notes 1. The hexadecimal numbers in the boxes show the display RAM address.
2. When 32 characters × 7 lines are displayed, set blank code "FF_{16}" to character code of addresses $E0_{16}$ to EF_{16}.

Fig. 4 Screen constitution (32 characters × 7 lines)

Display RAM DESCRIPTION

Display RAM Address 00_{16} to EF_{16}

DA 0~C	Name	Contents		Remarks
		Status	Function	
0	C0 (LSB)	0	Set ROM-held character code of a character needed to display.	
		①		
1	C1	0		
		①		
2	C2	0		
		①		
3	C3	0		
		①		
4	C4	0		
		①		
5	C5	0		
		①		
6	C6 (MSB)	0		
		①		
7	—	0	Set to “0” during normal operation	(Note 2)
		①	Can not be used	
8	R	0	When RGBON=1, set background color by character unit.	Refer to supplemental explanation (3).
		①		
9	G	0		
		①		
A	B	0		
		①		
B	BLINK	0	No blinking	Refer to BLINK2 to 0 (address $F5_{16}$)
		①	Blinking	
C	REV	⓪	Normal character	
		1	Reversed character	

Notes 1. Resetting at the $\overline{AC}$ pin RAM-erases the display RAM, and the status turns as indicated by the mark ◯ around in the status column.
2. Set to “1” only when setting a blank code. When using M35055-XXXFP, DA7 is C7 (MSB).

Display control register

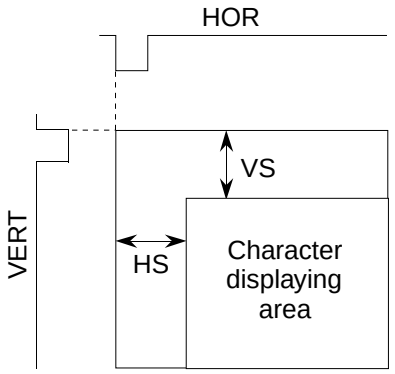
(1) Address F0$_{16}$

DA 0~D	Register	Contents: Status	Contents: Function	Remarks
0	PTC0	⓪	P0 output (port 0)	Port output control
		1	BLNK1 output	
1	PTC1	⓪	P1 output (port 1)	
		1	CO1 output	Refer to supplemental explanation (4).
2	PTD0	⓪	It is negative polarity at P0 output “L”, BLINK1 output.	Control the port data
		1	It is positive polarity at P0 output “H”, BLINK1 output.	
3	PTD1	⓪	It is negative polarity at P01 output “L”, CO1 output.	
		1	It is positive polarity at P01 output “H”, CO1 output.	Refer to supplemental explanation (4).
4	SEPV0	⓪	It should be fixed to “0”.	Specifies the vertical synchronous separation criterion
		1	Can not be used.	
5	SEPV1	⓪	It should be fixed to “0”.	
		1	Can not be used.	Refer to supplemental explanation (1).
6	SYSEP0	⓪		Specifies the sync-bias potential
		1		
7	SYSEP1	⓪		
		1		
8	TEST10	⓪	It should be fixed to “0”.	
		1	Can not be used.	
9	TEST11	⓪	It should be fixed to “0”.	
		1	Can not be used.	
A	TEST12	⓪	Can not be used.	
		1	It should be fixed to “1”.	
B	TEST13	⓪	It should be fixed to “0”.	
		1	Can not be used.	
C	TEST14	⓪	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST15	⓪	It should be fixed to “0”.	
		1	Can not be used.	

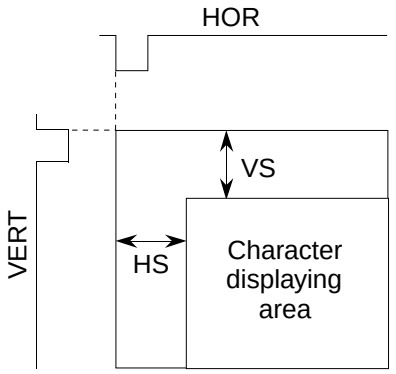
SYSEP1	SYSEP0	Bias potential
0	0	Can not be used.
0	1	Can not be used.
1	0	1.75V
1	1	Can not be used.

Note: The mark ◯ around the status value means the reset status by the “L” level is input to $\overline{AC}$ pin.

(2) Address F1$_{16}$

DA 0~D	Register	Contents: Status	Contents: Function	Remarks
0	HP0 (LSB)	⓪	Let horizontal display start position be HS, $HS = T \times (\sum_{n=0}^{7} 2^n HPn+6)$  T : The oscillation cycle of display clock	Set the horizontal display start position by use of HP7 through HP0. HP7 to HP0 = (00000000) to (00001111) setting is forbidden. It can be set this up to 240 steps in increments of one T.
		1		
1	HP1	⓪		
		1		
2	HP2	⓪		
		1		
3	HP3	⓪		
		1		
4	HP4	⓪		
		1		
5	HP5	⓪		
		1		
6	HP6	⓪		
		1		
7	HP7 (MSB)	⓪		
		1		
8	TEST16	⓪	Can not be used.	
		1	It should be fixed to “1”.	
9	TEST17	⓪	Can not be used.	
		1	It should be fixed to “1”.	
A	TEST18	⓪	Can not be used.	
		1	It should be fixed to “1”.	
B	TEST19	⓪	Can not be used.	
		1	It should be fixed to “1”.	
C	TEST20	⓪	Can not be used.	
		1	It should be fixed to “1”.	
D	TEST21	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(3) Address F2$_{16}$

DA 0~D	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	⓪	Let vertical display start position be VS, $VS = H \times \sum_{n=0}^{7} 2^n VPnVS$  H : The oscillation cycle of horizontal synchronous signal	Set the vertical display start position by use of VP7 through VP0. VP7 to VP0 = (00000000) to (00000110) setting is forbidden. It can be set this up to 249 steps in increments of one H. VP7 to VP0 = (00000000) to (00100011) setting is forbidden.
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7 (MSB)	⓪		
		1		
8	TEST22	⓪	Can not be used.	
		1	It should be fixed to “1”.	
9	TEST23	⓪	Can not be used.	
		1	It should be fixed to “1”.	
A	TEST24	⓪	Can not be used.	
		1	It should be fixed to “1”.	
B	TEST25	⓪	Can not be used.	
		1	It should be fixed to “1”.	
C	TEST26	⓪	Can not be used.	
		1	It should be fixed to “1”.	
D	TEST27	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(4) Address F3$_{16}$

<table>
<tr><th>DA
0~D</th><th>Register</th><th colspan="2">Contents</th><th>Remarks</th></tr>
<tr><th></th><th></th><th>Status</th><th>Function</th><th></th></tr>
<tr><td>0</td><td>HSZ10</td><td>⓪</td><td rowspan="5"><table><tr><th>HSZ11</th><th>HSZ10</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="5">Character size setting in the horizontal direction for the first line.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>1</td><td>HSZ11</td><td>⓪</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>2</td><td>HSZ20</td><td>⓪</td><td rowspan="5"><table><tr><th>HSZ21</th><th>HSZ20</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="5">Character size setting in the horizontal direction for the 2nd line to 10th line.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>3</td><td>HSZ21</td><td>⓪</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>4</td><td>VSZ10</td><td>⓪</td><td rowspan="5"><table><tr><th>VSZ11</th><th>VSZ10</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="5">Character size setting in the vertical direction for the first line.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>5</td><td>VSZ11</td><td>⓪</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>6</td><td>VSZ20</td><td>⓪</td><td rowspan="5"><table><tr><th>VSZ21</th><th>VSZ20</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="5">Character size setting in the vertical direction for the 2nd line to 10th line.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>7</td><td>VSZ21</td><td>⓪</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>8</td><td>TEST28</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="4"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>9</td><td>TEST29</td><td>⓪</td><td>It should be fixed to “0”.</td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>A</td><td>TEST30</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="4"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>B</td><td>TEST31</td><td>⓪</td><td>It should be fixed to “0”.</td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>C</td><td>TEST32</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>D</td><td>TEST33</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

(5) Address F4$_{16}$

DA 0~D	Register	Contents: Status	Contents: Function	Remarks
0	DSP0	⓪		Set the display mode of line 1.
		1		
1	DSP1	⓪		Set the display mode of line 2.
		1		
2	DSP2	⓪		Set the display mode of line 3.
		1		
3	DSP3	⓪		Set the display mode of line 4.
		1		
4	DSP4	⓪		Set the display mode of line 5.
		1		
5	DSP5	⓪		Set the display mode of line 6.
		1		
6	DSP6	⓪		Set the display mode of line 7.
		1		
7	DSP7	⓪		Set the display mode of line 8.
		1		
8	DSP8	⓪		Set the display mode of line 9.
		1		
9	DSP9	⓪		Set the display mode of line 10.
		1		
A	SPACE	⓪	Normal display	Put a space line between line 2 and line 3 in displaying 32 characters.
		1	Put a space line between line 2 and line 3, and between line 8 and line 9.	
B	TEST34	⓪	It should be fixed to “0”.	
		1	Can not be used.	
C	TEST35	⓪	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST36	⓪	It should be fixed to “0”.	
		1	Can not be used.	

BLK1	BLK0	DSPn= “1”	DSPn= “0”
0	0	Matrix-outline border size	Matrix-outline size
0	1	Border size	Character size
1	0	Matrix-outline size	Border size
1	1	Character size	Matrix-outline size

Depends on BLK0 and BLK1 (address F8$_{16}$)
DSPn in the generic name for DSP0 to DSP9.
DSP0 to DSP9 are each controlled independently.

(6) Address F5$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BLINK0</td><td>⓪</td><td rowspan="6"><table><tr><th>BLINK0</th><th>BLINK1</th><th>Duty</th></tr><tr><td>0</td><td>0</td><td>Blinking off</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="6">Blinking duty ratio can be altered. (Note)</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">BLINK1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">BLINK2</td><td>⓪</td><td>Division of vertical synchronizing signal into 1/64. Cycle approximately 1 second.</td><td rowspan="2">Blinking cycle can be altered.</td></tr>
<tr><td>1</td><td>Division of vertical synchronizing signal into 1/32. Cycle approximately 0.5 second.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">$\overline{N}$/P</td><td>⓪</td><td>NTSC, M-PAL mode</td><td rowspan="2">Refer to register MPAL</td></tr>
<tr><td>1</td><td>PAL mode</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">$\overline{INT}$/NON</td><td>⓪</td><td>Interlace</td><td rowspan="2">Scanning lines control (only in internal synchronization)</td></tr>
<tr><td>1</td><td>Non interlace</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">MPAL</td><td>⓪</td><td rowspan="2"><table><tr><th>$\overline{N}$/P</th><th>MPAL</th><th>Synchronous mode</th></tr><tr><td>0</td><td>0</td><td>NTSC</td></tr><tr><td>0</td><td>1</td><td>M-PAL</td></tr><tr><td>1</td><td>0</td><td>PAL</td></tr><tr><td>1</td><td>1</td><td>Not available</td></tr></table></td><td rowspan="2">Synchronizing signal is selected with this register and $\overline{N}$/P register.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">PALH</td><td>⓪</td><td rowspan="2"><table><tr><th>PALH</th><th>$\overline{INT}$/NON</th><th>Number of scanning lines</th></tr><tr><td rowspan="2">0</td><td>0</td><td>625H lines</td></tr><tr><td>1</td><td>626H lines</td></tr><tr><td rowspan="2">1</td><td>0</td><td>627H lines</td></tr><tr><td>1</td><td>628H lines</td></tr></table></td><td rowspan="2">It should be fixed to “0” at NTSC</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">EQP</td><td>⓪</td><td>Not include the equivalent pulse.</td><td rowspan="2">Effective only at non-interlace</td></tr>
<tr><td>1</td><td>Include the equivalent pulse.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">TEST37</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">TEST38</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST39</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST40</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">TEST41</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST42</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Note. To blink a character, set 1 to DAB (the blinking bit) of the display RAM.

(7) Address F6$_{16}$

<table>
<tr><th rowspan="2">DA
0~D</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PHASE0</td><td>⓪</td><td rowspan="9">
<table>
<tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>Raster</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>White</td></tr>
</table>
</td><td rowspan="9">Raster color setting
Refer to supplemental explanation (2) about video signal level</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PHASE1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PHASE2</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LEVEL0</td><td>⓪</td><td>Internal bias off</td><td rowspan="2">Generates bias potential for composite video signals</td></tr>
<tr><td>1</td><td>Internal bias on</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BR</td><td>⓪</td><td rowspan="9">
<table>
<tr><th>BB</th><th>BG</th><th>BR</th><th>Character back-ground color</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>White</td></tr>
</table>
</td><td rowspan="9">Character background color setting.
Refer to supplemental explanation (2) about video signal level</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BG</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BB</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BLKHF</td><td>⓪</td><td>The halftone displaying “OFF” in superimpose</td><td rowspan="2">This register is available in the superimpose displaying only. (Note)</td></tr>
<tr><td>1</td><td>The halftone displaying “ON” in superimpose</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">LIN$\overline{24}$/32</td><td>⓪</td><td>24 characters × 10 lines display</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>32 characters × 7 lines display</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">LBLACK</td><td>⓪</td><td>Blanking level Ⅰ 2.3V</td><td rowspan="2">Set a blackness level</td></tr>
<tr><td>1</td><td>Blanking level Ⅱ 2.1V</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST0</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST1</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">TEST2</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST43</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should to be fixed to “1”.</td></tr>
</table>

Note. It is neccessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200Ω register in series.

(8) Address F7$_{16}$

DA 0~D	Register	Contents		Remarks
		Status	Function	
0	CUR0	⓪	Let cursor displaying address be CURS, $CURS = \sum_{n=0}^{7} 2^n CURn$	Set the cursor displaying address by use of CUR7 through CUR0. CUR7 to CUR0 (11110000) setting is forbidden under 24 characters display. CUR7 to CUR0 (11100000) setting is forbidden under 32 characters display. Set CUR7 to CUR0 = (11111111) under cursor is not be displayed. The cursor displaying address (CURS) is correspond to display construction.
		1		
1	CUR1	⓪		
		1		
2	CUR2	⓪		
		1		
3	CUR3	⓪		
		1		
4	CUR4	⓪		
		1		
5	CUR5	⓪		
		1		
6	CUR6	⓪		
		1		
7	CUR7	⓪		
		1		
8	CBLINK	⓪	No blinking	The cursor blinking setting
		1	Blinking	
9	CL$\overline{17}$/18	⓪	Cursor displaying at the 17th dot by vertical direction.	Refer to character construction.
		1	Cursor displaying at the 18th dot by vertical direction.	
A	TEST44	⓪	It should be fixed to “0”.	
		1	Can not be used.	
B	RGBON	⓪	Normal	Refer to supplemental explanation (3).
		1	Character background coloring	
C	TEST45	⓪	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST46	⓪	It should be fixed to “0”.	
		1	Can not be used.	

(9) Address F8$_{16}$

<table>
<tr><th>DA
0~D</th><th>Register</th><th colspan="2">Contents</th><th>Remarks</th></tr>
<tr><th></th><th></th><th>Status</th><th>Function</th><th></th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BLK0</td><td>⓪</td><td rowspan="5"><table><tr><th>BLK1</th><th>BLK0</th><th>DSPn= “1”</th><th>DSPn= “0”</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline border size</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Border size</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Matrix-outline size</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Character size</td><td>Matrix-outline size</td></tr></table></td><td rowspan="5">Display mode
(BLNK output) variable</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">BLK1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>⓪</td><td>External synchronization</td><td rowspan="2">Synchronizing signal switching (Note1)</td></tr>
<tr><td>1</td><td>Internal synchronization</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SCOR</td><td>⓪</td><td>Superimpose monotone display</td><td rowspan="2">“1” setting is forbidden at internal synchronous or PAL, M-PAL mode displaying.</td></tr>
<tr><td>1</td><td>Superimpose coloring display (only NTSC)</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">STOPIN</td><td>⓪</td><td>fSC input mode</td><td rowspan="2">OSCIN oscillation control</td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">STOP1</td><td>⓪</td><td>Oscillation VCO for display</td><td rowspan="2">Control oscillation VCO for display</td></tr>
<tr><td>1</td><td>Stop oscillation VCO for display</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">DSPON</td><td>⓪</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">RAMERS</td><td>⓪</td><td>RAM not erased</td><td rowspan="2">This register does not exist (Note 3).</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">TEST47</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">TEST48</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST49</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST50</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">TEST51</td><td>⓪</td><td>Can not be used.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>It should be fixed to “1”.</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">LEVEL1</td><td>⓪</td><td>Internal bias OFF</td><td rowspan="2">Generates bias potential for synchronous separation.</td></tr>
<tr><td>1</td><td>Internal bias ON</td></tr>
</table>

Notes 1. In dealing with the internal synchronization, cut off external video signals outside the IC. The leakage of external input video signals can be avoided.

2. In displaying color superimposition, enter into the OSCIN pin the fSC signal that phase-synchronizes with the color burst of the composite video signals (input to the CVIN pin).

3. Erases all the display RAM. The character code turns to blank-FF$_{16}$, the encode data bit and the blinking bit turn to “1” respectively, and reversed character bit turns to “0”.

Supplemental explanation about display control register

(1) How to effect synchronous separation from composite video signals

Synchronous separation is effected as follows depending on the width of L-level of the vertical synchronous period.

1. Less than 8.4μs …… Not to be determined to be a vertical synchronous signal.
2. Equal to or higher than 8.4μs but less than 15.6μs …… When two clocks continue, if take place, it is "L" period is determined to be a vertical synchronization signal.
3. Equal to or higher than 15.6μs …… It is "L" period is determined to be a vertical synchronous signal with no condition.

The determination is made at the timing indicated by V in Fig.4 either in case 2 or in case 3.

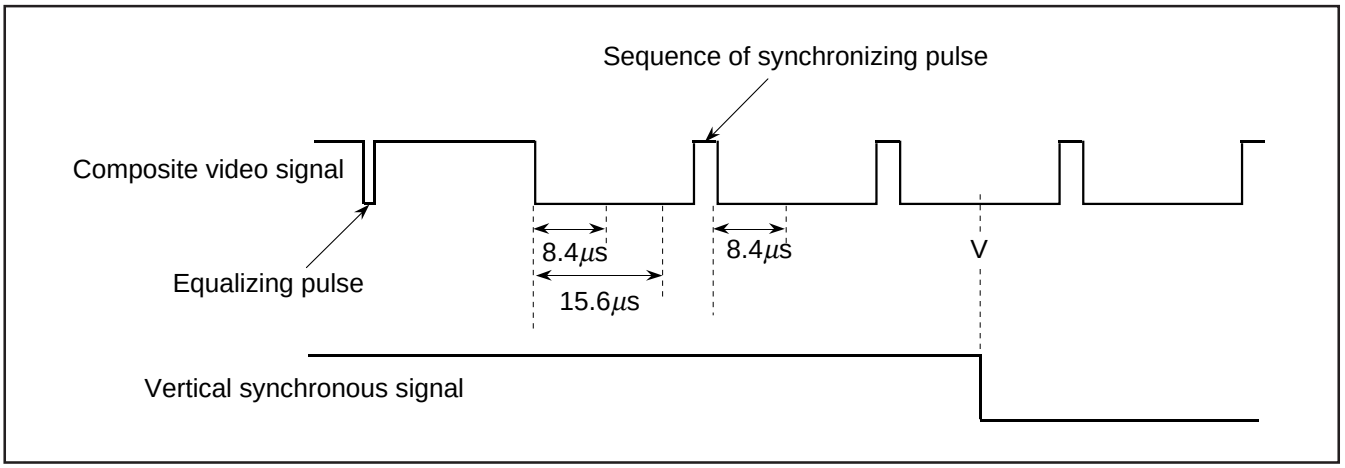
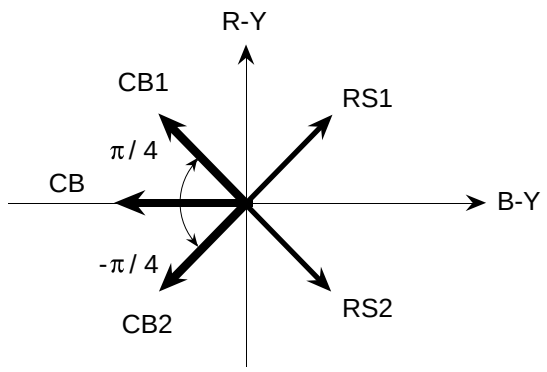


Fig. 5 The method of synchronous separation from composite video signal.

(2) Video signal level

V_{DD} : 5.0V, Ta : 25°C

Color	Phase angle (rad)		Brightness level (V)			Amplitude ratio (to color burst)		
	NTSC method	PAL, M-PAL method	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync-chip	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color burst	0	$\pm 4\pi/16$	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red	$7\pi/16 \pm 2\pi/16$	$\pm 7\pi/16 \pm 2\pi/16$	2.3	2.5	2.7	1.5	3.0	4.5
Green	$27\pi 16 \pm 2\pi/16$	$\mp 5\pi/16 \pm 2\pi/16$	2.7	2.9	3.1	1.4	2.8	4.2
Yellow	$\pi/16 \pm 2\pi/16$	$\pm \pi/16 \pm 2\pi/16$	3.1	3.3	3.5	1.0	2.0	3.0
Blue	$17\pi/16 \pm 2\pi/16$	$\mp 15\pi/16 \pm 2\pi/16$	2.0	2.2	2.4	1.0	2.0	3.0
Magenta	$11\pi/16 \pm 2\pi/16$	$\pm 11\pi/16 \pm 2\pi/16$	2.5	2.7	2.9	1.4	2.8	4.2
Cyan	$23\pi/16 \pm 2\pi/16$	$\mp 9\pi/16 \pm 2\pi/16$	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—



CB ··· Color burst under NTSC
CB1,CB2 ··· Color burst under PAL or M-PAL
RS1,RS2 ··· Color subcarrier under PAL or M-PAL

Fig. 6 Bector phases

(3) Setting RGBON (address $F7_{16}$)

RGBON = "0" ..... Sets background colors depending on BB, BG, and BR (address $F6_{16}$), screen by screen.
RGBON = "1" ..... Sets background colors depending on R, G, B (address 00_{16} to EF_{16}), character by character. The color setting is shown below.

Color Setting

B	G	R	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

(4) Port output and BLNK1, CO1 output

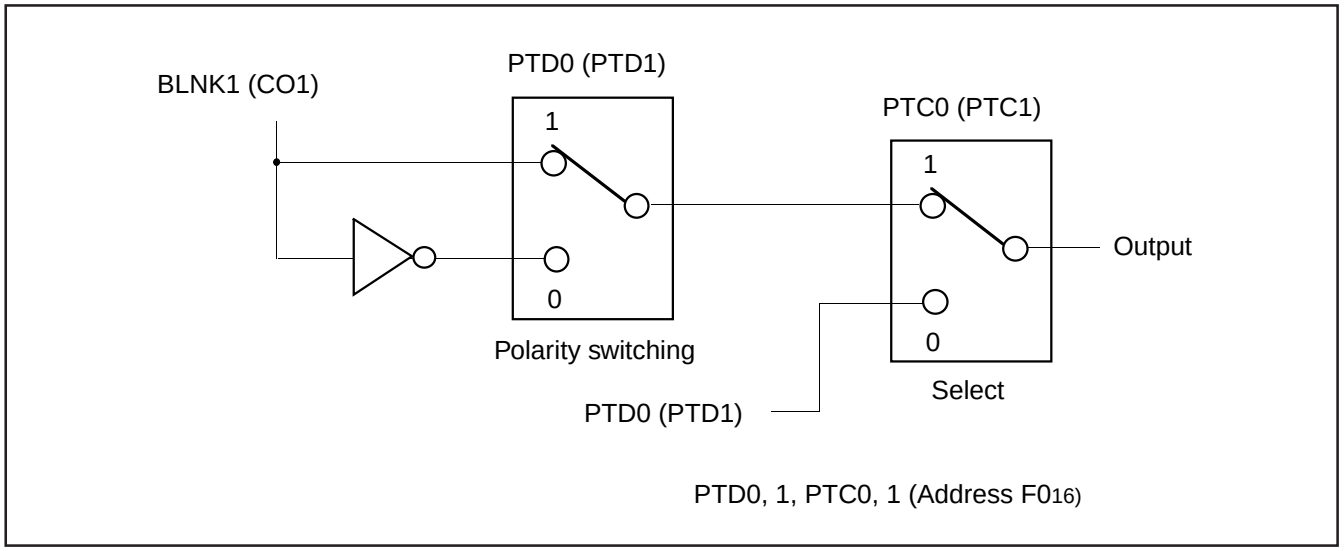


Fig. 7 Example of port control

(5) Setting conditions for oscillating or stopping the display clock

	at display clock operating	at display clock stop
STOP1	0	1
DSPON	1	0
CS pin	L	H

STOP1, CDSPON (Address $F8_{16}$)

(6) Setting condition at LEVEL0,1

	Operation state (Character display)		Now-working condition (no characters are displayed)
	Internal synchronous	External synchronous	
LEVEL0	1	1	0
LEVEL1	0	1	0

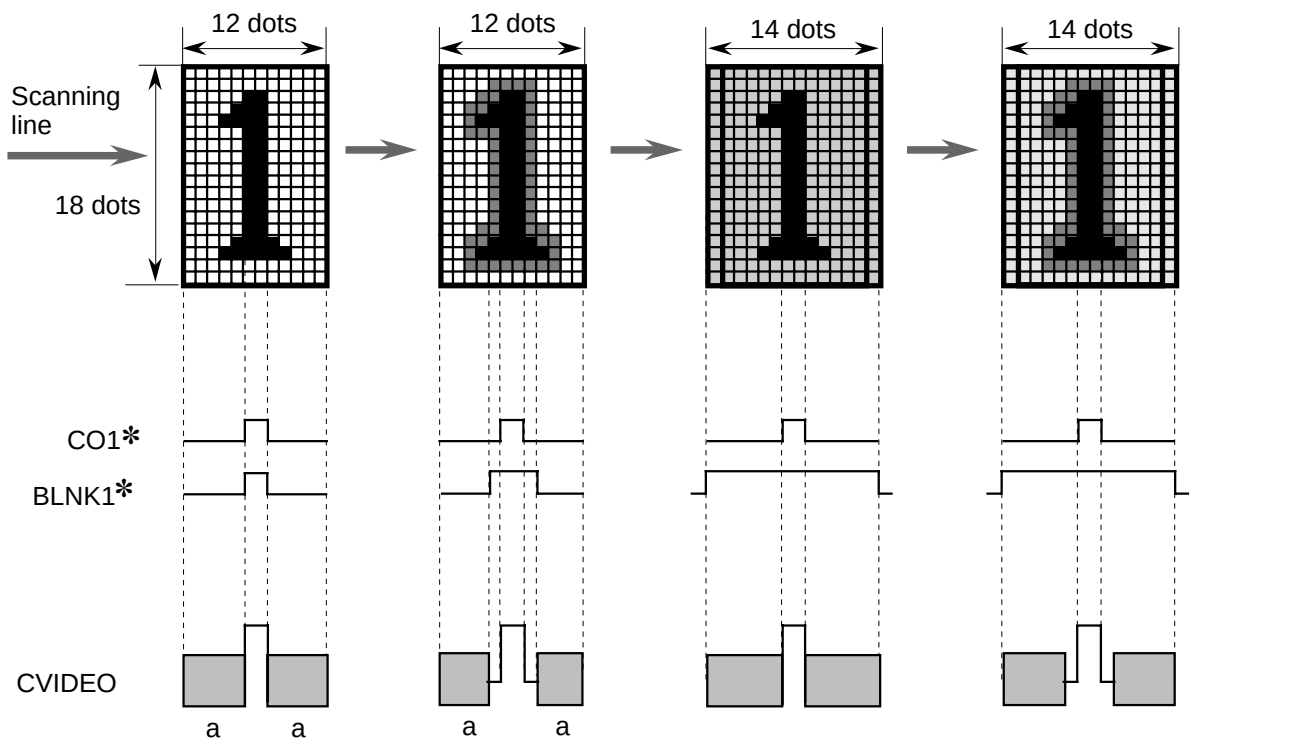
LEVEL0 (address $F6_{16}$), LEVEL1 (address $F8_{16}$)

DISPLAY FORMS

M35054-XXXFP/M35055-XXXFP have the following four display forms as the blanking function, when CO1 and BLNK1 are output.

(1) Character size : Blanking same as the character size.
(2) Border size : Blanking the background as a size from character.
(3) Matrix-outline size: Blanking the background as a size from all character font size.
(4) Matrix-outline border size : Blanking the background as a size from all character font size. Border display.

This display format allows each line to be controlled independently, so that two kinds of display formats can be combined on the same screen.



(1) Character size (2) Border size (3) Matrix-outline size (4) Matrix-outline border size

Note: In this case, the output polarity that CO1 * and BLNK1* is positive.

a: Background carrier color signal

Fig. 8 Display forms at each display mode

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by then serial input function.
Owing to automatic address increment, not necessary to enter addresses for the second and subsequent data.
In automatically, the next of address $F8_{16}$ is assigned to address 00_{16}.
Fig. 9 shows an example of data setting by the serial input function (M35054-XXXFP), Fig. 10 shows an example of data setting by the serial input function (M35055-XXXFP).

NO.	Data contewts		DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/Data	Spplemental explanation																
1	Address($F8_{16}$)	Address setting	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
2	Data($F8_{16}$)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Data(00_{16})	Display RAM address 00_{16} to EF_{16} setting	0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
4	Data(01_{16})		0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
~	~						~								~			
241	Data(EE_{16})		0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
242	Data(EF_{16})		0	0	0	REV	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
243	Data($F0_{16}$)	Register address $F0_{16}$ to $F7_{16}$ setting	0	0	0	0	0	1	0	0	1	0	0	0	PTD 1	PTD 0	PTC 1	PTC 0
244	Data($F1_{16}$)		0	0	0	1	1	1	1	1	HP 7	HP 6	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
245	Data($F2_{16}$)		0	0	0	1	1	1	1	1	VP 7	VP 6	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
246	Data($F3_{16}$)		0	0	0	0	0	0	0	0	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data($F4_{16}$)		0	0	0	0	0	SPACE	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data($F5_{16}$)		0	0	0	0	0	0	0	0	EQP	PALH	MPAL	$\overline{INT}$ /NON	$\overline{N}$/P	BLINK 2	BLINK 1	BLINK 0
249	Data($F6_{16}$)		0	0	1	TEST 2	TEST 1	TEST 0	LBLACK	LIN $\overline{24}$/32	BLKHF	BB	BG	BR	LEVEL 0	PHASE 2	PHASE 1	PHASE 0
250	Data($F7_{16}$)		0	0	0	0	RGBON	0	CL $\overline{17}$/18	CBLINK	CURS 7	CURS 6	CURS 5	CURS 4	CURS 3	CURS 2	CURS 1	CURS 0
251	Data($F8_{16}$)	Display ON	0	0	LEVEL 1	1	1	1	1	1	RAM ERS	DSPON	STOP 1	STOP IN	SCOR	EX	BLK 1	BLK 0

Fig. 9 Example of data setting by the serial input function (M35054-XXXFP)

NO.	Data couteuts		DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/Data	Supplemental explauation																
1	Address($F8_{16}$)	Address setting	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
2	Data($F8_{16}$)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Data(00_{16})	Display RAM address 00_{16} to EF_{16} setting	0	0	0	REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
4	Data(01_{16})		0	0	0	REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
≀	≀						≀							≀				
241	Data(EE_{16})		0	0		REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
242	Data(EF_{16})		0	0	0	REV	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
243	Data($F0_{16}$)	Register address $F0_{16}$ to $F7_{16}$ setting	0	0	0	0	0	1	0	0	1	0	0	0	PTD 1	PTD 0	PTC 1	PTC 0
244	Data($F1_{16}$)		0	0	0	1	1	1	1	1	HP 7	HP 6	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
245	Data($F2_{16}$)		0	0	0	1	1	1	1	1	VP 7	VP 6	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
246	Data($F3_{16}$)		0	0	0	0	0	0	0	0	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data($F4_{16}$)		0	0	0	0	0	SPACE	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data($F5_{16}$)		0	0	0	0	0	0	0	0	EQP	PALH	MPAL	$\overline{\text{INT}}$ /NON	$\overline{\text{N}}$/P	BLINK 2	BLINK 1	BLINK 0
249	Data($F6_{16}$)		0	0	1	TEST 2	TEST 1	TEST 0	LBLACK	$\overline{\text{LIN}}$ 24/32	BLKHF	BB	BG	BR	LEVEL 0	PHASE 2	PHASE 1	PHASE 0
250	Data($F7_{16}$)		0	0	0	0	RGBON	0	$\overline{\text{CL}}$ 17/18	CBLINK	CURS 7	CURS 6	CURS 5	CURS 4	CURS 3	CURS 2	CURS 1	CURS 0
251	Data($F8_{16}$)	Display ON	0	0	LEVEL 1	1	1	1	1	1	RAM ERS	DSPON	STOP 1	STOP IN	SCOR	EX	BLK 1	BLK 0

Fig. 10 Example of data setting by the serial input function (M35055-XXXFP)

SERIAL DATA INPUT TIMING

(1) The address consists of 16 bits.
(2) The data consists of 16 bits.
(3) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

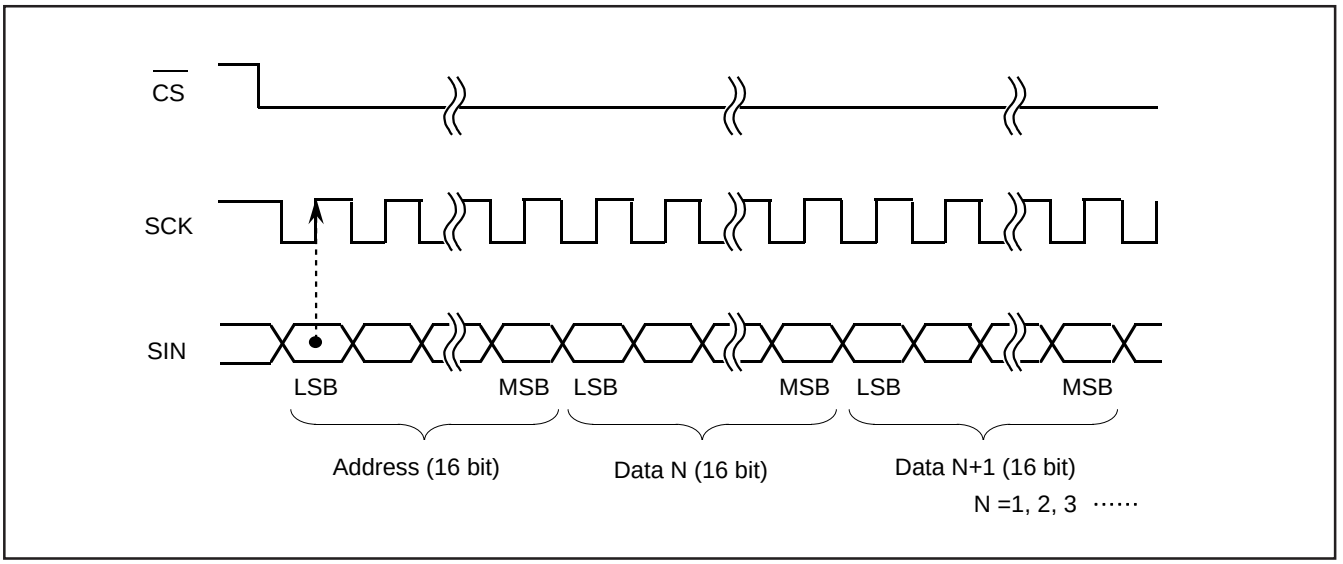


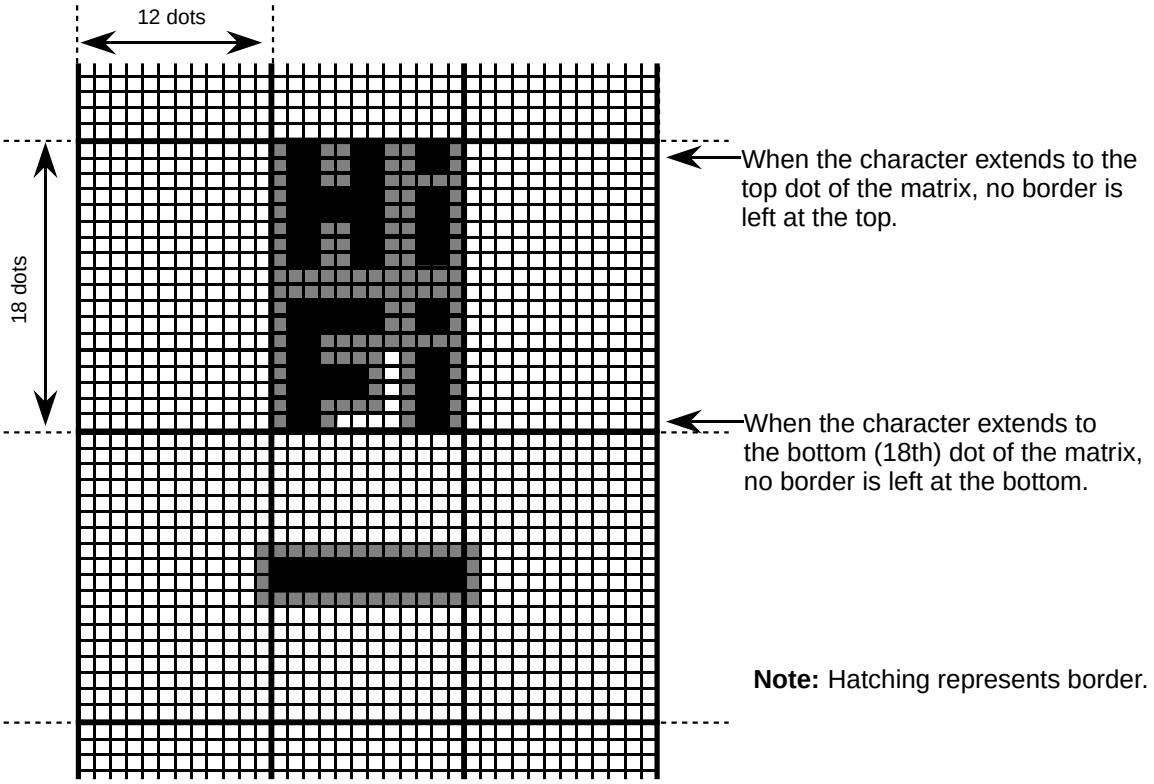
Fig. 11 Serial input timing

CHARACTER FONT

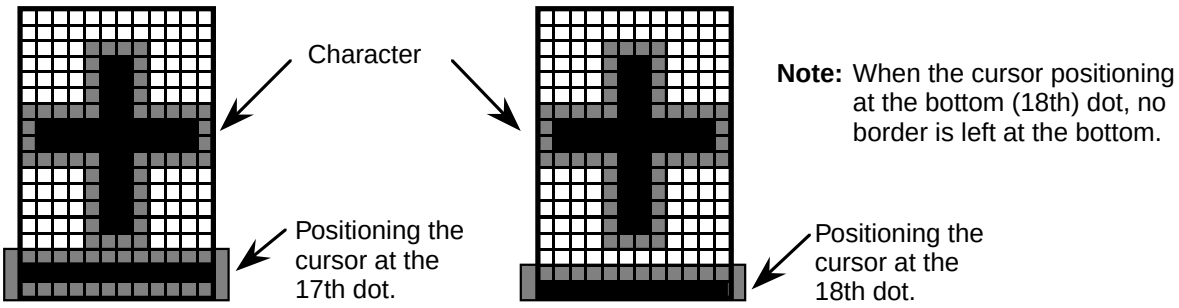
Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code "FF16" is so fixed as to be blank and to have no background, thus cannot assign a character font to this code.

(1) Border display (set by register BLK0, 1 (address F816))



(2) Cursor display (Border display)



Register CL$\overline{17}$/18 (address F716) = "0" Register CL$\overline{17}$/18 ="0"

Fig. 12 Character font and border

M35054-XXXFP/M35055-XXXFP PERIPHERAL CIRCUIT

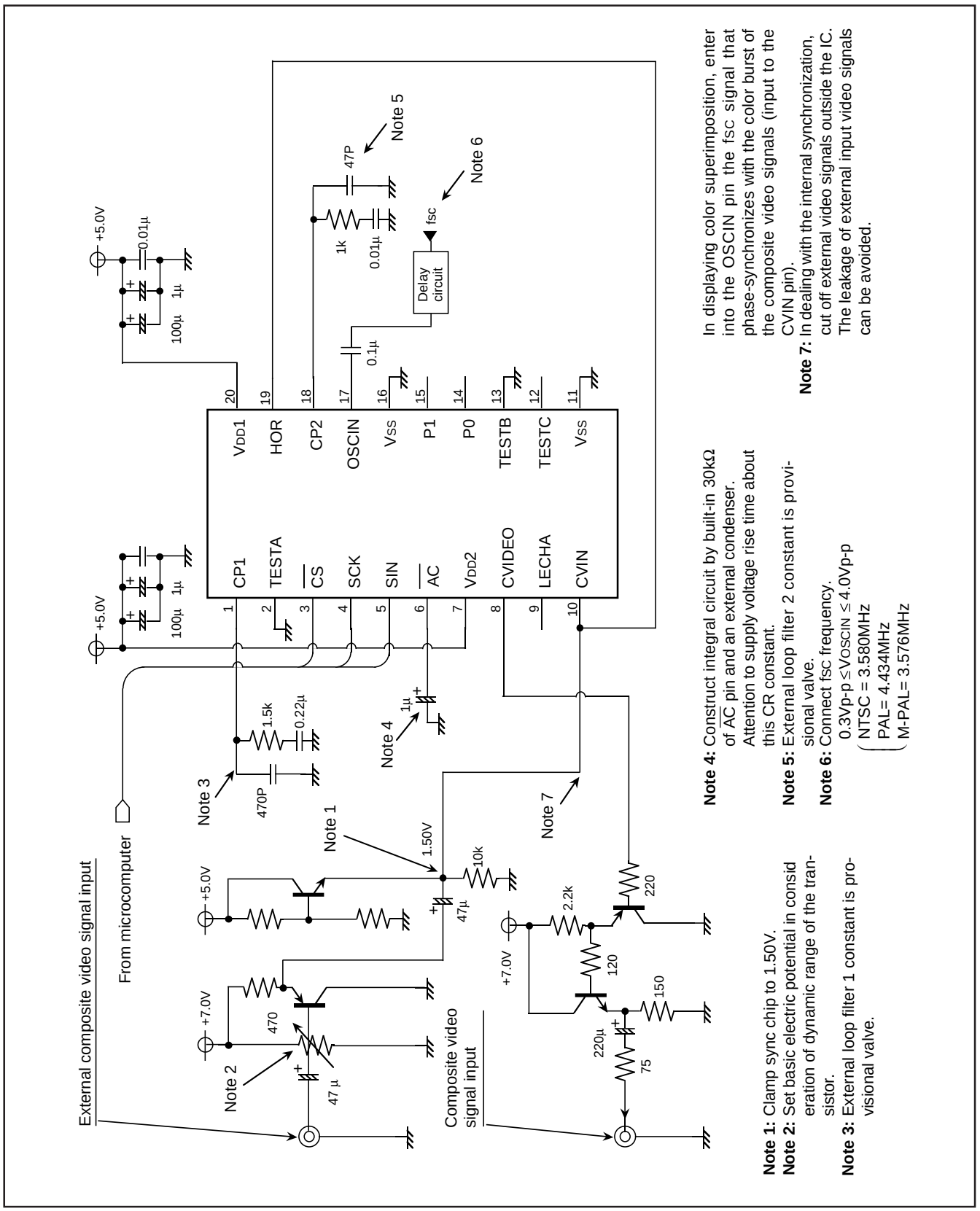


Fig. 13 M35054-XXXFP/M35055-XXXFP example of peripheral circuit

Precautions

(1) Points to note in setting the display RAMs

a) Be careful to the edges may sway depending on the combination of character's background color and raster color.

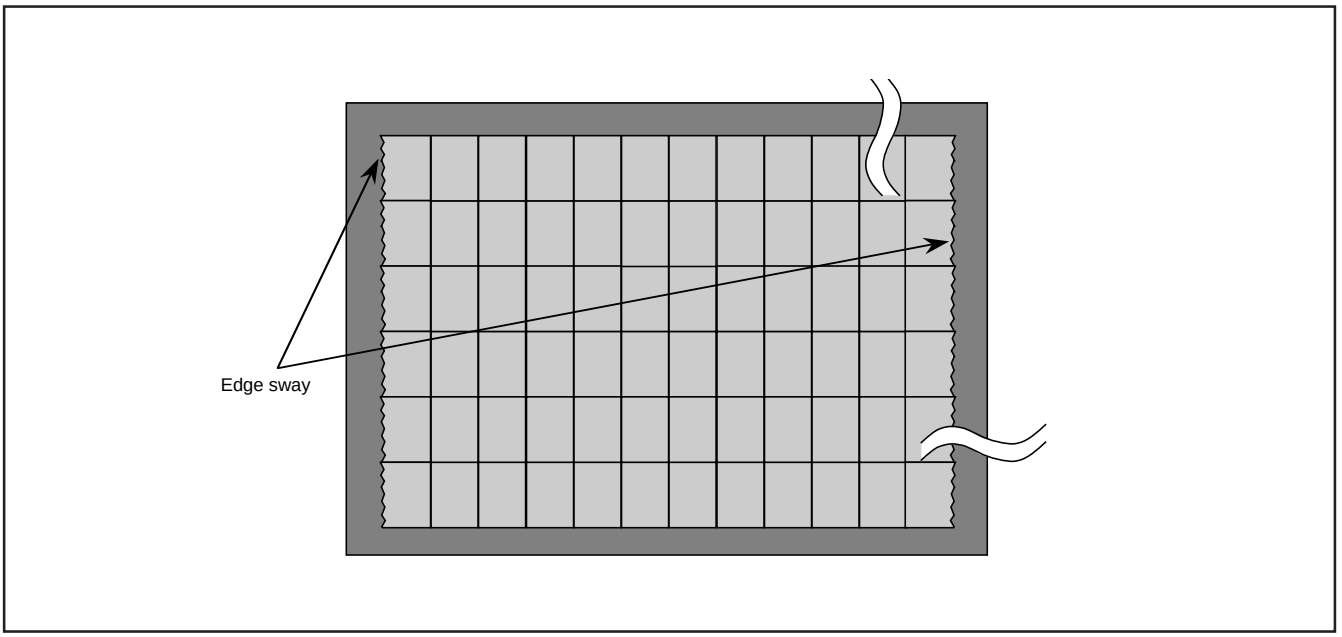


Fig. 14 Example of display

b) If what display exceeds the display area in dealing with external synchronization, (if use double - size characters), set the character code of the addresses lying outside that display area blank code – "FF16".

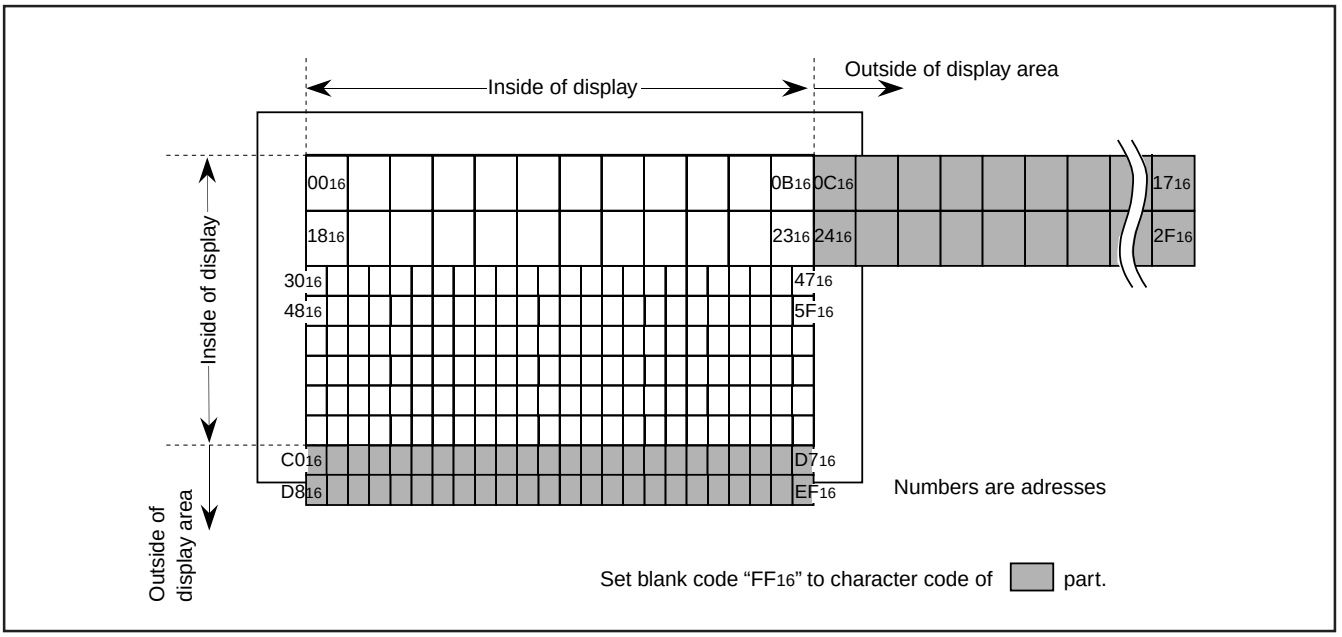


Fig. 15 Example of display

(2) Before setting registers at the starting of system, be sure to reset the M35052-XXXSP/FP by applying "L" level to the $\overline{AC}$ pin.

(3) Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

(4) Synchronous correction action

When switching channel or in the special playback mode (quick playback, rewinding, and so on) of VTR, effect of synchronous correction becomes strong, and distortion of a character is apt to occur because the continuity of video signal is suddenly switched. When the continuity of video signal is out of order, erasure of displayed characters is recommended in a extreme short time to raise the quality of displayed characters.

(5) Notes on fSC signal input

This IC amplifies the subcarrier frequency (fSC) signal (NTSC, M-PAL system: 3.58MHz, PAL system: 4.43MHz) input to the OSCIN pin (17-pin) and generates the composite video signal internally. The amplified fSC signal can be destabilized in the following cases.

a) When the fSC signal is outside of recommended operating conditions.

b) When the waveform of the fSC signal is distorted.

c) When DC level in the fSC waveform fluctuates.

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(6) Forbidding to stop entering the fSC signal

This IC doesn't properly work if the fSC signal is not entered into the OSCIN pin (pin 17), so don't stop the fSC signal so as to work the IC. To stop the IC, turn the display off (set 0 in the register DSPON (address $F8_{16}$).)

(7) Forbidding to set data during the period in which the internal oscillation circuit stabilizes

a) To start entering the fSC signal when its input is stopped.

b) To start oscillating the oscillation circuit for display when its oscillation is stopped. (to assign "1" to the register STOP1 (address $F8_{16}$) when it is assigned "0", or the like.)

c) To turn on the internal bias when it is turned off. (to assign "1" to the register LEVEL1 (address $F8_{16}$) when it is assigned "0".)

There can be instances in which data are not properly set in the registers until the internal oscillation circuit stabilizes, so follow the steps in sequence as given below.

1) Set "0" in the register DSPON (address $F8_{16}$). (the display is turned off)
2) Effect the settings a), b), and c) given above.
3) Wait 20 ms (the period necessary for the internal oscillation circuit to stabilize) before entering data.
4) Set necessary data in other registers, and make the display RAM ready.

TIMING REQUIREMENTS (Ta = –20°C to 70°C, V_{DD} = 5±0.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(SCK)	SCK width	400	—	—	ns
tsu($\overline{CS}$)	$\overline{CS}$ setup time	200	—	—	ns
th($\overline{CS}$)	$\overline{CS}$ hold time	2	—	—	μs
tsu(SIN)	SIN setup time	200	—	—	ns
th(SIN)	SIN hold time	200	—	—	ns
t_{word}	1 word writing time	12.8	—	—	μs

Note. When oscillation stop at register STOR1 (address $F8_{16}$), 1V (field term) or more of t_{SU}($\overline{CS}$) and th($\overline{CS}$) are needed.

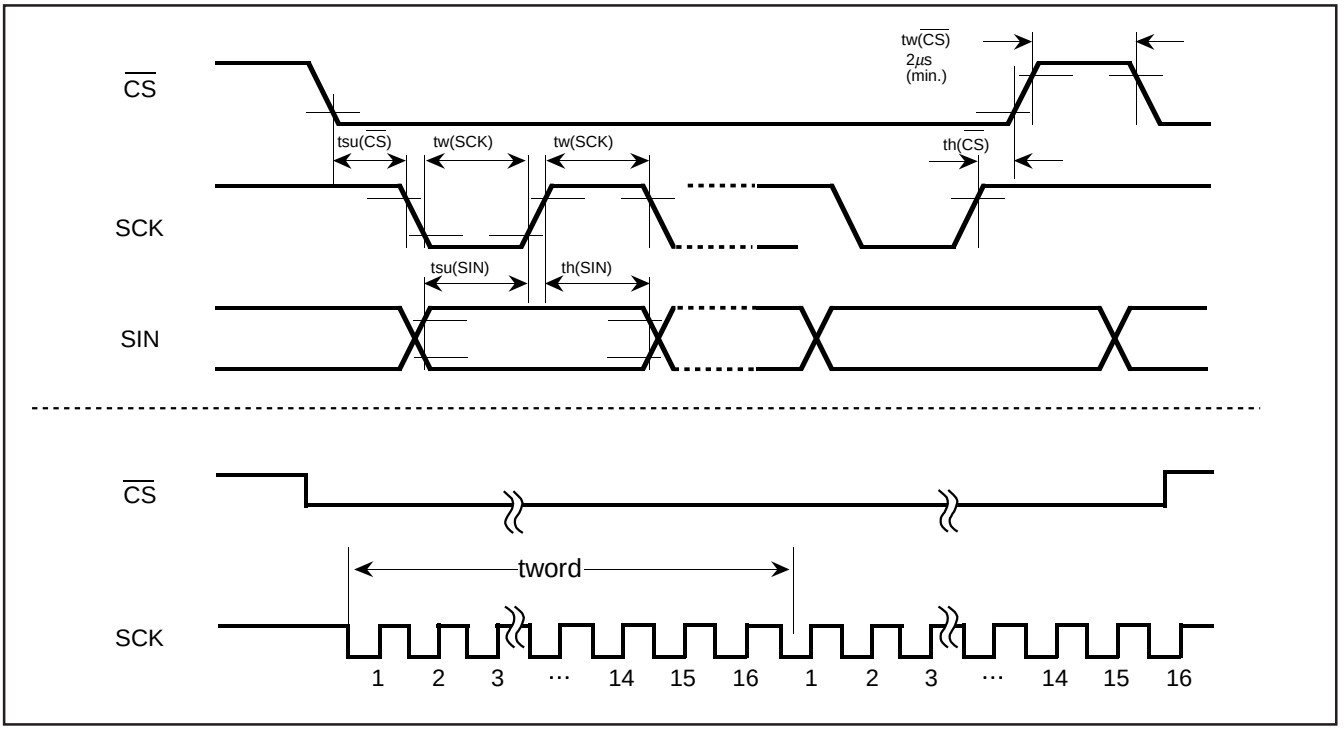


Fig. 16 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	–0.3~6.0	V
V_I	Input voltage		V_{SS}–0.3≤V_I≤V_{DD}+0.3	V
V_O	Output voltage		V_{SS}≤V_O≤V_{DD}	V
P_d	Power dissipation	Ta=25°C	300	mW
T_{opr}	Operating temperature		–20~70	°C
T_{stg}	Storage temperature		–40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.75	5.00	5.25	V
V_{IH}	"H"level input voltage $\overline{AC}$, $\overline{CS}$, SIN, SCK, TESTA, TESTB		0.8×V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage $\overline{AC}$, $\overline{CS}$, SIN, SCK, TESTA, TESTB		0	0	0.2×V_{DD}	V
V_{CVIN}	CVIN, HOR		–	2.0V_{P-P}	–	V
V_{OSCIN}	Input voltage OSCIN (Note)		0.3V_{P-P}	–	4.0V_{P-P}	V
f_{OSCIN}	Synchronous signal oscillation frequency (Duty 40~60%)		–	3.580 4.434 3.576	–	MHz
f_{OSC1}	Display oscillation frequency	24 characters×10 lines	–	480×f_H	–	MHz
f_{OSC2}		32 characters×7 lines	–	640×f_H	–	MHz

Notes 1. Noise component is within 30mV.
2. f_H: Horizontal synchronous frequency (MHz).

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Ta=–20~70°C	4.75	5.00	5.25	V
I_{DD}	Supply current	V_{DD}=5.00V	–	30	50	mA
V_{OH}	"H"level output voltage P0, P1	V_{DD}=4.75V, I_{OH}=–0.4mA	3.75	–	–	V
V_{OL}	"L" level output voltage P0, P1	V_{DD}=4.75V, I_{OL}=0.4mA	–	–	0.4	V
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$, SCK, SIN, TESTB	V_{DD}=5.00V	10	30	100	kΩ

VIDEO SIGNAL INPUT CONDITIONS (V_{DD} = 5V, Ta = –20 to 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IN-SC}	Composite video signal input clamp voltage	Sync-chip voltage	–	1.5	–	V

Note for Supplying Power

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35054-XXXFP/ M35055-XXXFP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 16. tw is the interval after the supply voltage becomes 0.8 × VDD or more and before the supply voltage to the $\overline{AC}$ pin ($V_{\overline{AC}}$) becomes 0.2 × VDD or more. After supplying the power (VDD and VSS) to M35054-XXXFP/ M35055-XXXFP, the tw time must be reserved for 1ms or more. Before starting input from the microcomputer, the waiting time (ts) must be reserved for 500ms after the supply voltage to the $\overline{AC}$ pin becomes 0.8 × VDD or more.

(2) Timing of power supplying to VDD1 pin and VDD2 pin

The power need to supply to VDD1 and VDD2 at a time, though it is separated perfectly between the VDD1 as the digital line and the VDD2 as the analog line.

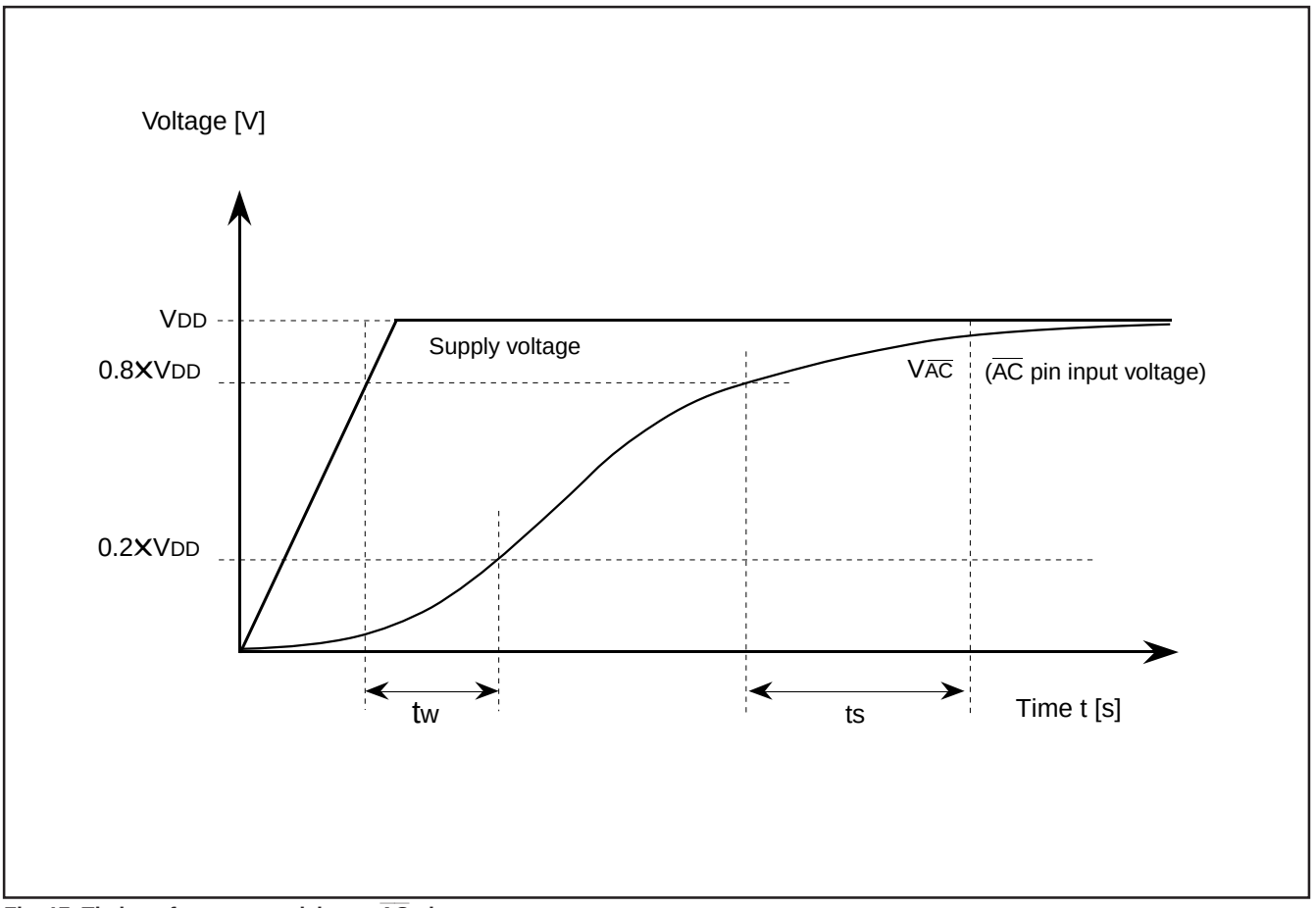


Fig. 17 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

Connect a capacitor (approx. 0.1 ˚F) between pins VDD and VSS at the shortest distance using relatively thick wire to prevent noise and latch up.

ROM ORDERING METHOD

Please submit the information described below when ordering Mask ROM.

(1) ROM Order Confirmation Form 1
(2) Data to be written into mask ROM ..... EPROM (three sets containing the identical data)
(3) Mark Specification Form 1
(4) Program for character font generating + froppy disk in which character data is input

STANDARD ROM TYPE : M35054-001FP

M35054-001FP is a standard ROM type of M35054-XXXFP character patterns are fixed to the contents of Figure 18 to 19.

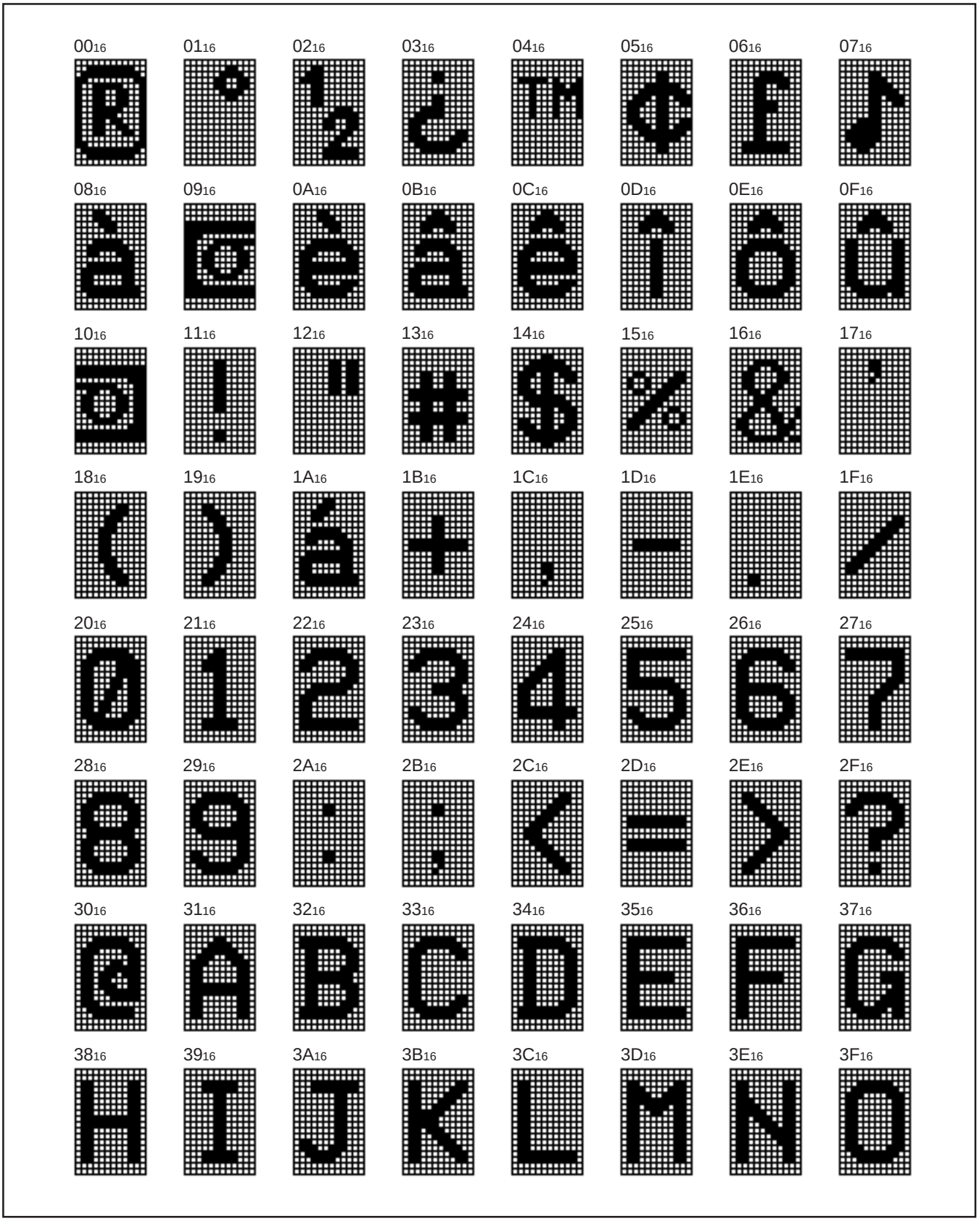


Fig. 18 M35054-001FP character pattern (1)

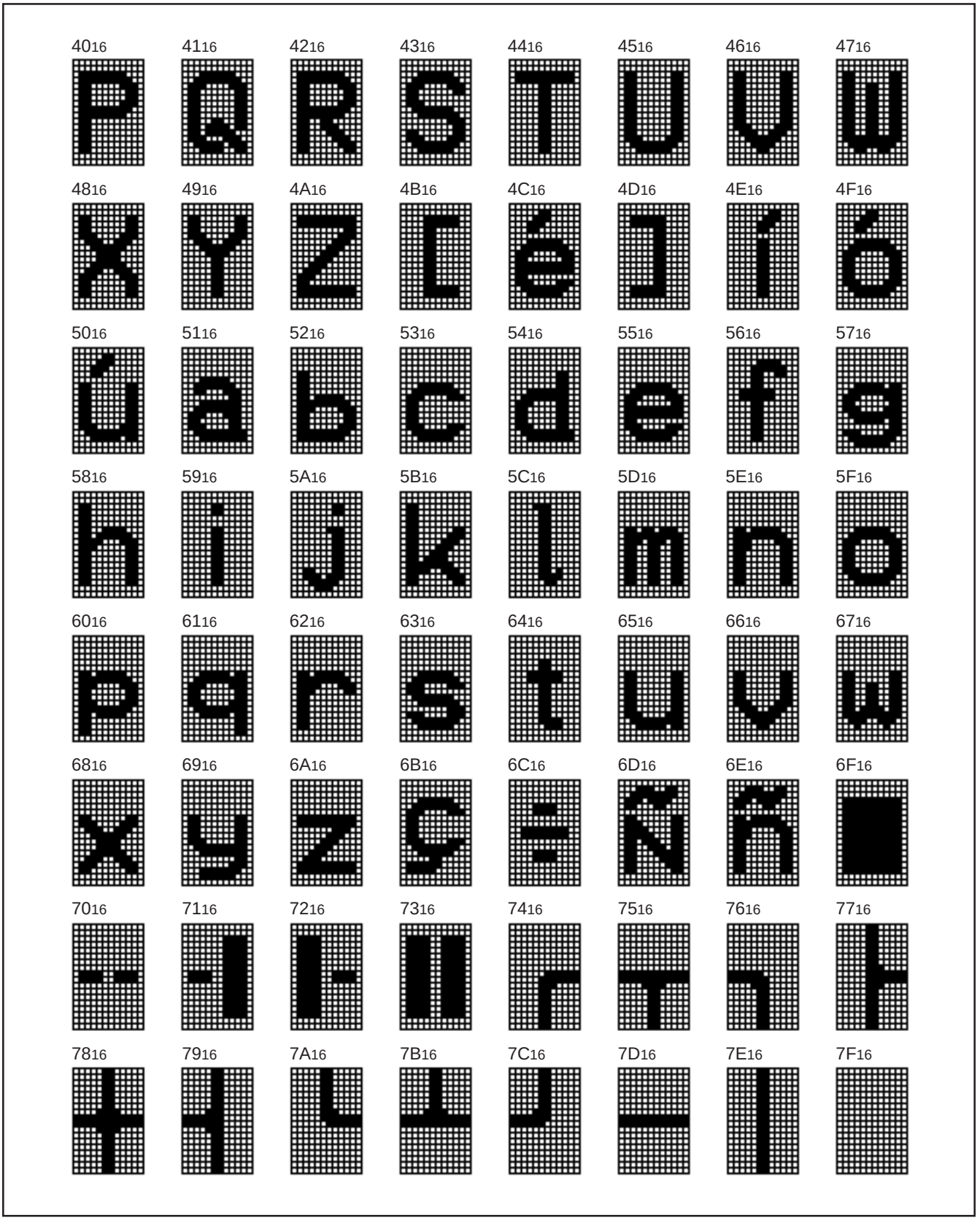


Fig. 19 M35054-001FP character pattern (2)

STANDARD ROM TYPE : M35055-001FP

M35055-001FP is a standard ROM type of M35055-XXXFP
Character patterns are fixed to the contents of Figure 20 to 23.

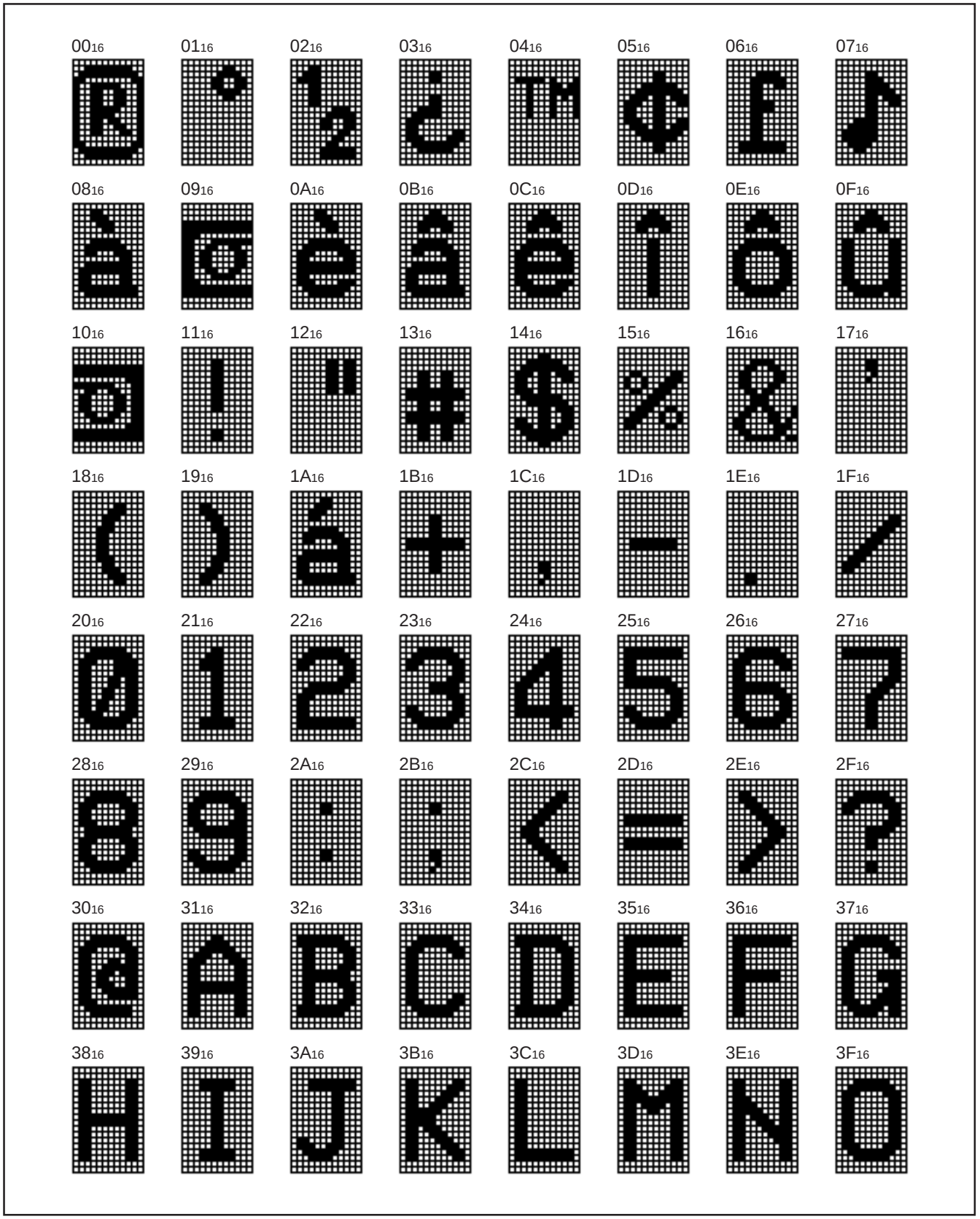


Fig. 20 M35055-001FP character pattern (1)

Fig. 21 M35055-001FP character pattern (2)

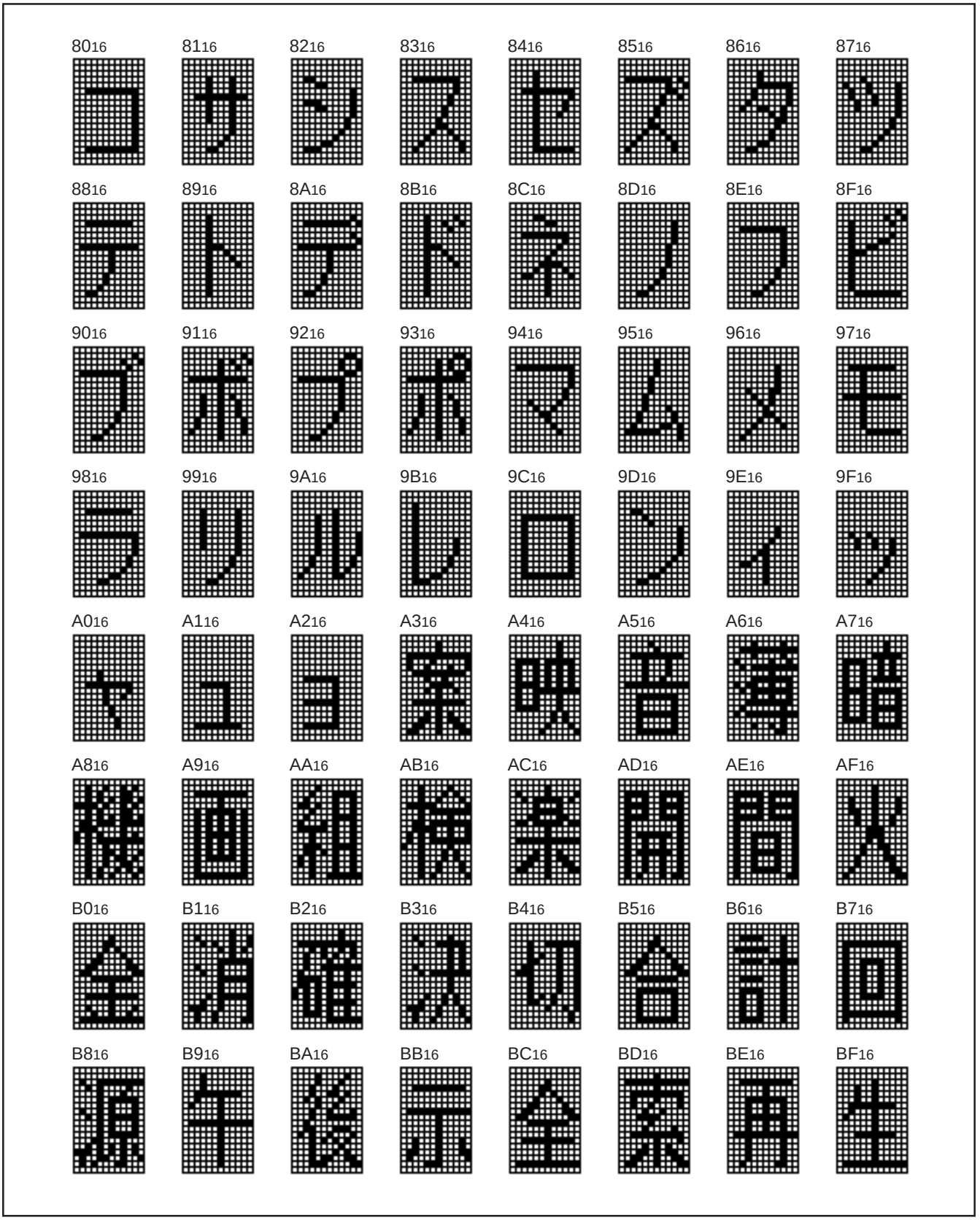


Fig. 22 M35055-001FP character pattern (3)

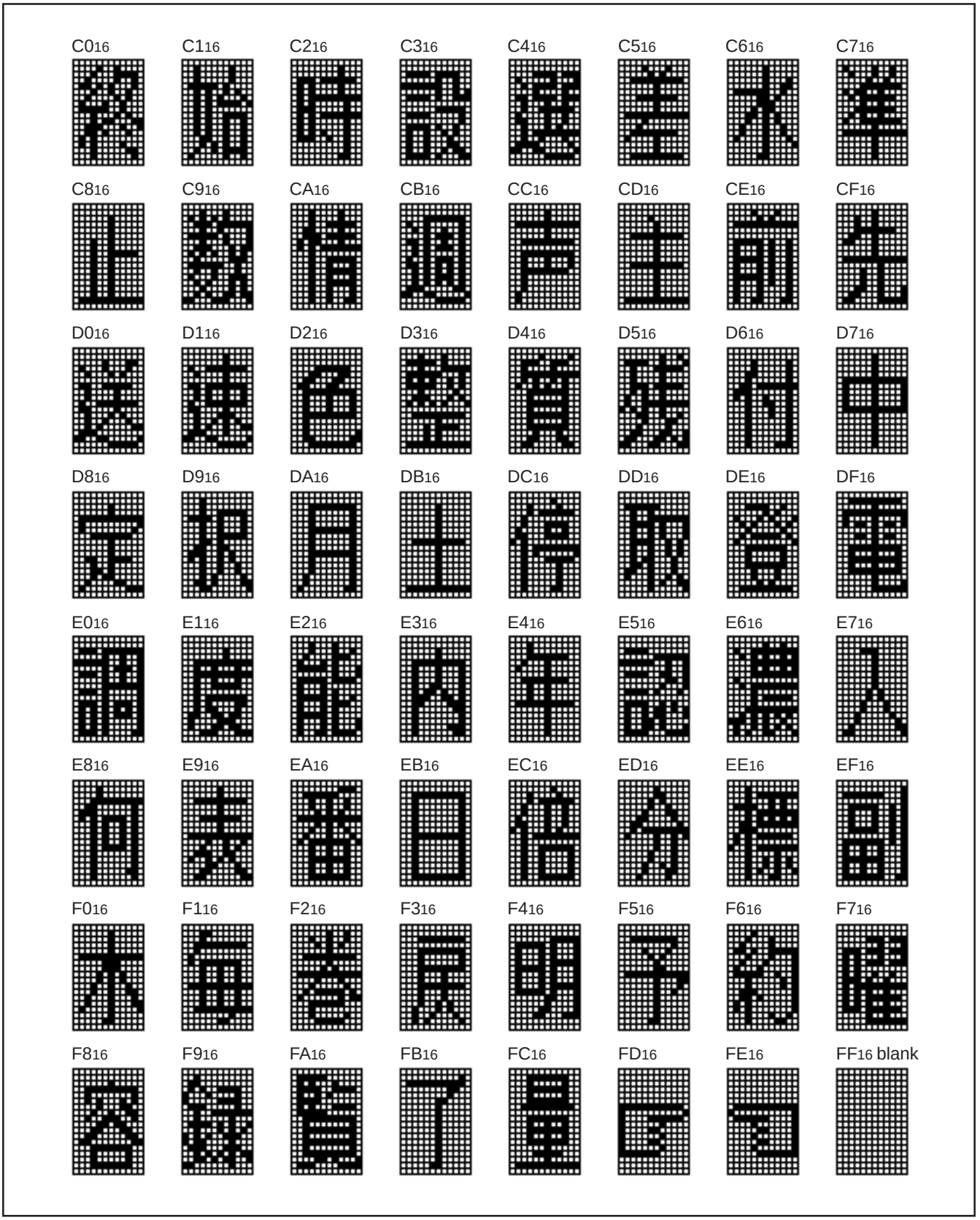


Fig. 23 M35055-001FP character pattern (4)

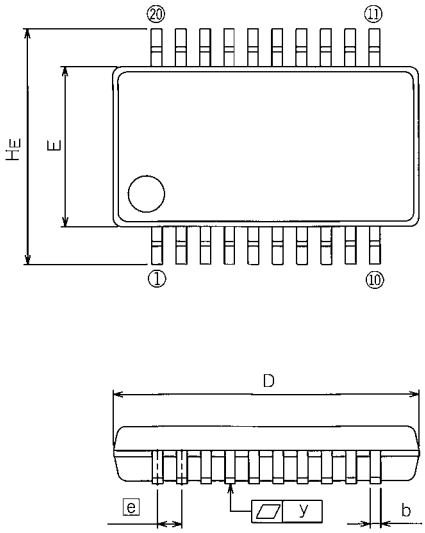
PACKAGE OUTLINE

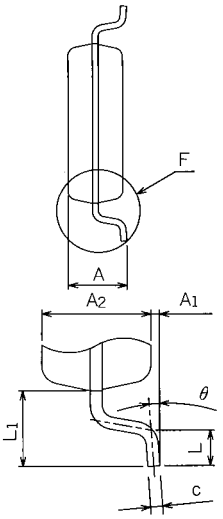
20P2Q−A

Plastic 20pin 300mil SSOP

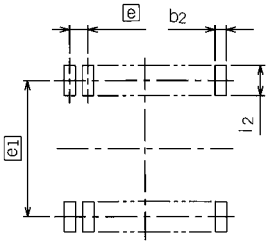
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP020-P-0300	−	0.2	Cu Alloy

Scale : 4/1





Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	−	−	2.1
A_1	0	0.1	0.2
A_2	−	1.8	−
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	−	0.8	−
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	−	1.25	−
y	−	−	0.1
θ	0°	−	8°
b_2	−	0.5	−
e_1	−	7.62	−
l_2	1.27	−	−

M35054-XXXFP/M35055-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST	M35054-XXXFP/M35055-XXXFP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980402
1.1	P48 20P2Q-A (20-PIN SSOP) MARK SPECIFICATION FORM B: Note 4 added	000707
1.2	Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM	000829